In the Claims

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1. (Currently amended) A digital signal processor (DSP), comprising:

a hardware accelerator; and

a parameter RAM coupled to said hardware accelerator, said parameter RAM adapted to exclusively store data for populating variables of programming instructions ~~operating condition parameters~~ for use in programming instructions stored elsewhere and used by said hardware accelerator.

2. (Original) The DSP as set forth in claim 1, wherein said parameter RAM comprises a 1K x 16 bit RAM.

3. (Original) The DSP as set forth in claim 1, wherein said DSP is used in connection with a communication system employing plural ADSL lines, and wherein said parameter RAM is configurable to store operating condition parameters for each of said plurality of ADSL lines.

4. (Original) The DSP as set forth in claim 3, wherein said parameter RAM is selectively configurable to store operating conditions for up to at least eight ADSL lines.

5. (Original) The DSP as set forth in claim 3, wherein said parameter RAM is selectively configurable to allocate sufficient memory per ADSL line to support each ADSL line employed.

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6. (Original) The DSP as set forth in claim 1, wherein said DSP is used in connection with a communication system employing plural ADSL lines, and wherein said parameter RAM is configured to store operating condition parameters for each of said plurality of ADSL lines.

7. (Original) The DSP as set forth in claim 6, wherein said parameter RAM is selectively configured to store operating conditions for up to at least eight ADSL lines.

8. (Original) The DSP as set forth in claim 6, wherein said parameter RAM is selectively configured to allocate sufficient memory per ADSL line to support each ADSL line employed.